Amendments to the Claims

1. (*Currently Amended*) A test access architecture for testing modules ~~(3)~~ in an electronic circuit, the test access architecture comprising:

[[-]] ~~the test access mechanism~~ a test access mechanism arranged to transport test stimulus data to, and test response data from a module ~~(3)~~ being tested;

[[-]] a global enable signal ~~(27)~~, the global enable signal ~~(27)~~ provided for placing the modules ~~(3)~~ in a test mode; and

[[-]] a control circuit ~~(59)~~ provided between the global enable signal ~~(27)~~ and an associated module ~~(3)~~, wherein the control circuit ~~(59)~~ is arranged to control whether or not the global enable signal ~~(27)~~ is passed to its associated module ~~(3)~~.

2. (*Currently Amended*) ~~A test access architecture as claimed in claim 1,~~ The test access architecture as recited in claim 1, wherein the control circuit ~~(59)~~ is controlled by a dedicated bypass signal ~~(61)~~ for that module.

3. (*Currently Amended*) ~~A test access architecture as claimed in claim 2,~~ The test access architecture as recited in claim 2, wherein the control circuit ~~(59)~~ is connected to receive the global enable signal ~~(27)~~ and the dedicated bypass signal ~~(61)~~, and arranged to provide a local enable signal ~~(60)~~ to its associated module ~~(3)~~ based on the respective states of the global enable signal ~~(27)~~ and the dedicated bypass signal ~~(61)~~.

4. (*Currently Amended*) ~~A test access architecture as claimed in claim 3,~~ The test access architecture as recited in claim 3, wherein the control circuit ~~(59)~~ is arranged to pass the global enable signal ~~(27)~~ if its associated module ~~(3)~~ is being tested, and to block the global enable signal ~~(27)~~ if its associated module ~~(3)~~ is not being tested.

5. (*Currently Amended*) ~~A test access architecture as claimed in any one of the preceding claims,~~ The test access architecture as recited in claim1, wherein the control circuit ~~(59)~~ is an OR gate.

6. (*Currently Amended*) ~~A test access architecture as claimed in any one of claims 1 to 4,~~ The test architecture as recited in claim 1, wherein the control circuit ~~(59)~~ is an AND gate.

7. (*Currently Amended*) ~~A test access architecture as claimed in claim 1,~~ The test architecture as recited in claim 1, wherein the electronic circuit is an integrated circuit.

8. (*Currently Amended*) ~~A test access architecture as claimed in claim 7,~~ The test architecture as recited in claim 7, wherein the control circuit ~~(59)~~ is located within a test wrapper of its associated module.

9. (*Currently Amended*) ~~A test access architecture as claimed in claim 7,~~ The test architecture as recited in claim 7, wherein the control circuit ~~(59)~~ is located in a test control block of a system on chip (SOC).

10. (*Currently Amended*) ~~A test access architecture as claimed in claim 1,~~ The test architecture as recited in claim 1, further comprising means for loading test stimulus data and unloading test response data in a pipelined manner.

11. (*Currently Amended*) ~~A test access architecture as claimed in claim 1,~~ The test architecture as recited in claim 1, wherein the global enable signal ~~(27)~~ is global to the test access mechanism (TAM) to which the plurality of modules ~~(3)~~ are connected.

12. (*Currently Amended*) ~~A test access architecture as claimed in claim 1,~~ The test architecture as recited in claim 1, wherein the global enable signal ~~(27)~~ is global to more than one test access mechanism (TAM) on the electronic circuit.

13. (*Currently Amended*) A method of testing a module ~~(3)~~ in an electronic circuit, the module ~~(3)~~ being one of a plurality of modules connected in series to a test access mechanism (TAM), the test access mechanism arranged to transport test stimulus data to

a module ~~(3)~~ being tested, and to transport test response data from the module ~~(3)~~ being tested, the method comprising the steps of:

[[-]] loading a first set of test stimulus data into the module ~~(3)~~ being tested;

[[-]] testing the module in response to a global enable signal ~~(27)~~ being activated;

[[-]] unloading test response data captured from the module ~~(3)~~ being tested; wherein, during the testing step, other modules ~~(3)~~ connected to the test access mechanism (TAM) are placed in a transport mode of operation, such that the other modules ~~(3)~~ do not corrupt a second set of test stimulus data being loaded into, or previous test response data being unloaded from, the module ~~(3)~~ under test.

14. (*Currently Amended*) ~~A method as claimed in claim 13,~~ The method as recited in claim 13, further comprising the step of providing a control circuit ~~(59)~~ between the global enable signal ~~(27)~~ and an associated module ~~(3)~~, wherein the control circuit ~~(59)~~ is arranged to control whether or not the global enable signal ~~(27)~~ is passed to its associated module ~~(3)~~.

15. (*Currently Amended*) ~~A method as claimed in claim 14,~~ The method as recited in claim 14, wherein the control circuit ~~(59)~~ is controlled by a dedicated bypass signal ~~(61)~~.

16. (*Currently Amended*) ~~A method as claimed in claim 15,~~ The method as recited in claim 15, wherein the control circuit ~~(59)~~ is connected to receive the global enable signal ~~(27)~~ and the dedicated bypass signal ~~(61)~~, and arranged to provide a local enable signal ~~(60)~~ to its associated module ~~(3)~~ based on the respective states of the global enable signal ~~(27)~~ and the dedicated bypass signal ~~(61)~~.

17. (*Currently Amended*) ~~A method as claimed in claim 16,~~ The method as recited in claim 16, wherein the control circuit ~~(59)~~ is arranged to pass the global enable signal ~~(27)~~ if its associated module ~~(3)~~ is being tested, and to block the global enable signal ~~(27)~~ if its associated module ~~(3)~~ is to be placed in the transport mode.

18. (*Currently Amended*) ~~A method as claimed in claim 13,~~ The method as recited in claim 13, comprising the step of providing an OR logic function as the control circuit (59).

19. (*Currently Amended*) ~~A method as claimed in claim 13,~~ The method as recited in claim 13,, comprising the step of providing an AND logic function as the control circuit ~~(59)~~.

20. (*Currently Amended*) ~~A method as claimed in claim 13,~~ The method as recited in claim 13, further comprising the step of providing the control circuit (59) within a test wrapper of its associated module ~~(3)~~.

21. (*Currently Amended*) ~~A method as claimed in claim 13,~~ The method as recited in claim 13, further comprising the step of providing the control circuit (59) in a test control block of a system on chip (SOC).

22. (*Currently Amended*) ~~A method as claimed in claim 15,~~ The method as recited in claim 15, further comprising the step of providing the control circuit ~~(59)~~ within its associated module ~~(3)~~.

23. (*Currently Amended*) ~~A method as claimed in claim 13,~~ The method as recited in claim 13, wherein the test pattern data is processed in a pipelined manner, such that modules located prior to the module ~~(3)~~ being tested contain the next set of test stimulus data from a series of test stimulus data, and modules located after the module ~~(3)~~ to be tested contain test response data from previous tests.

24. (*Currently Amended*) ~~A method as claimed in claim 13,~~ The method as recited in claim 13, wherein the global enable signal ~~(27)~~ is arranged to be global to the test access mechanism (TAM) to which the plurality of modules ~~(3)~~ are connected.

25. (*Currently Amended*) ~~A method as claimed in claim 13,~~ The method as recited in claim 13, wherein the global enable signal ~~(27)~~ is arranged to be global to more than one test access mechanism (TAM) on the electronic circuit.